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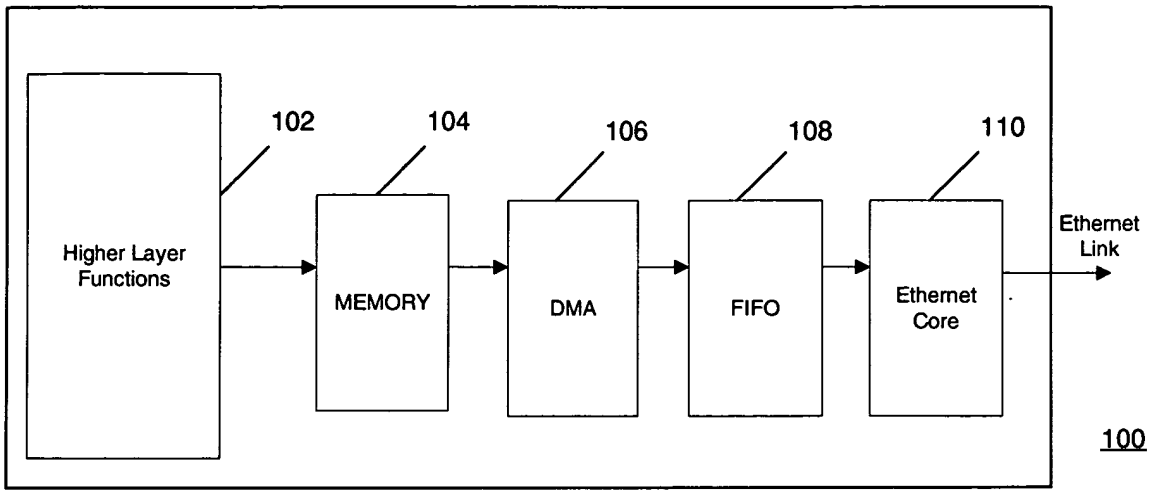

FIG. 1

	Byte Lane 0	Byte Lane 1	Byte Lane 2	Byte Lane 3	Byte Lane 4	Byte Lane 5	Byte Lane 6	Byte Lane 7
X00h	x	x	x	0	1	2	3	4
X08h	5	6	7	8	9	10	11	12
X10h	13	14	15	16	17	18	19	20
X18h	21	22	23	24	25	26	27	28
X18h	29	30	31	x	x	x	x	x

FIG. 2

	Byte Lane 0	Byte Lane 1	Byte Lane 2	Byte Lane 3	Byte Lane 4	Byte Lane 5	Byte Lane 6	Byte Lane 7
X00h	0	1	2	3	4	5	6	7
X08h	8	9	10	11	12	13	14	15
X10h	16	17	18	19	20	21	22	23
X18h	24	25	26	27	28	29	30	31

FIG. 3

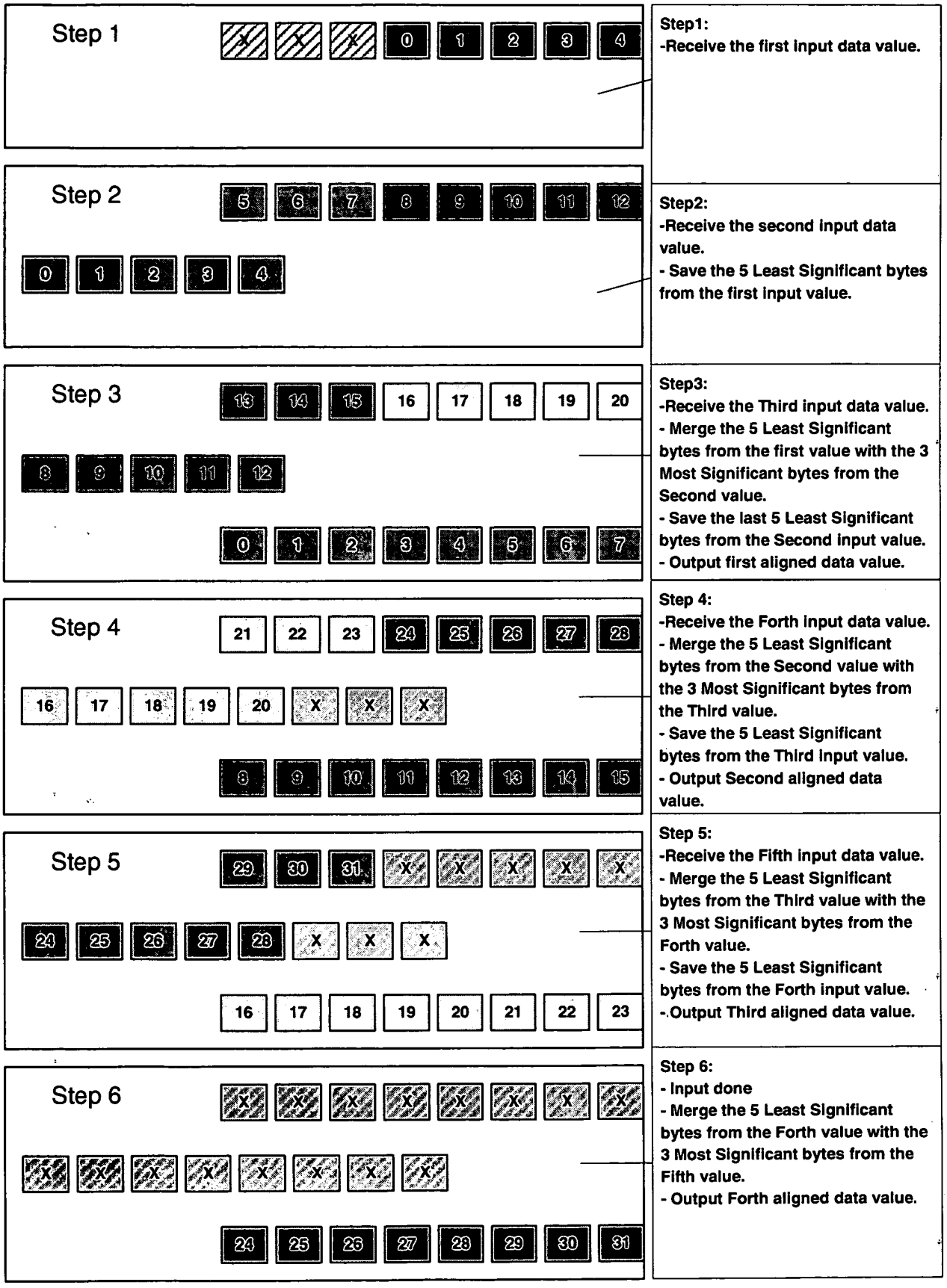
Step 1
X X X 0 1 2 3 4
Step1:
-Receive the first input data value.
Step 2
5 6 7 8 9 10 11 12
0 1 2 3 4
Step2:
-Receive the second input data value.
- Save the 5 Least Significant bytes from the first input value.
Step 3
13 14 15 16 17 18 19 20
8 9 10 11 12
0 1 2 3 4 5 6 7
Step3:
-Receive the Third input data value.
- Merge the 5 Least Significant bytes from the first value with the 3 Most Significant bytes from the Second value.
- Save the last 5 Least Significant bytes from the Second input value.
- Output first aligned data value.
Step 4
21 22 23 24 25 26 27 28
16 17 18 19 20 X X X
8 9 10 11 12 13 14 15
Step 4:
-Receive the Forth input data value.
- Merge the 5 Least Significant bytes from the Second value with the 3 Most Significant bytes from the Third value.
- Save the 5 Least Significant bytes from the Third input value.
- Output Second aligned data value.
Step 5
29 30 31 X X X X X
24 25 26 27 28 X X X
16 17 18 19 20 21 22 23
Step 5:
-Receive the Fifth input data value.
- Merge the 5 Least Significant bytes from the Third value with the 3 Most Significant bytes from the Forth value.
- Save the 5 Least Significant bytes from the Forth input value.
-.Output Third aligned data value.
Step 6
X X X X X X X X
X X X X X X X X
24 25 26 27 28 29 30 31
Step 6:
- Input done
- Merge the 5 Least Significant bytes from the Forth value with the 3 Most Significant bytes from the Fifth value.
- Output Forth aligned data value.

FIG. 4

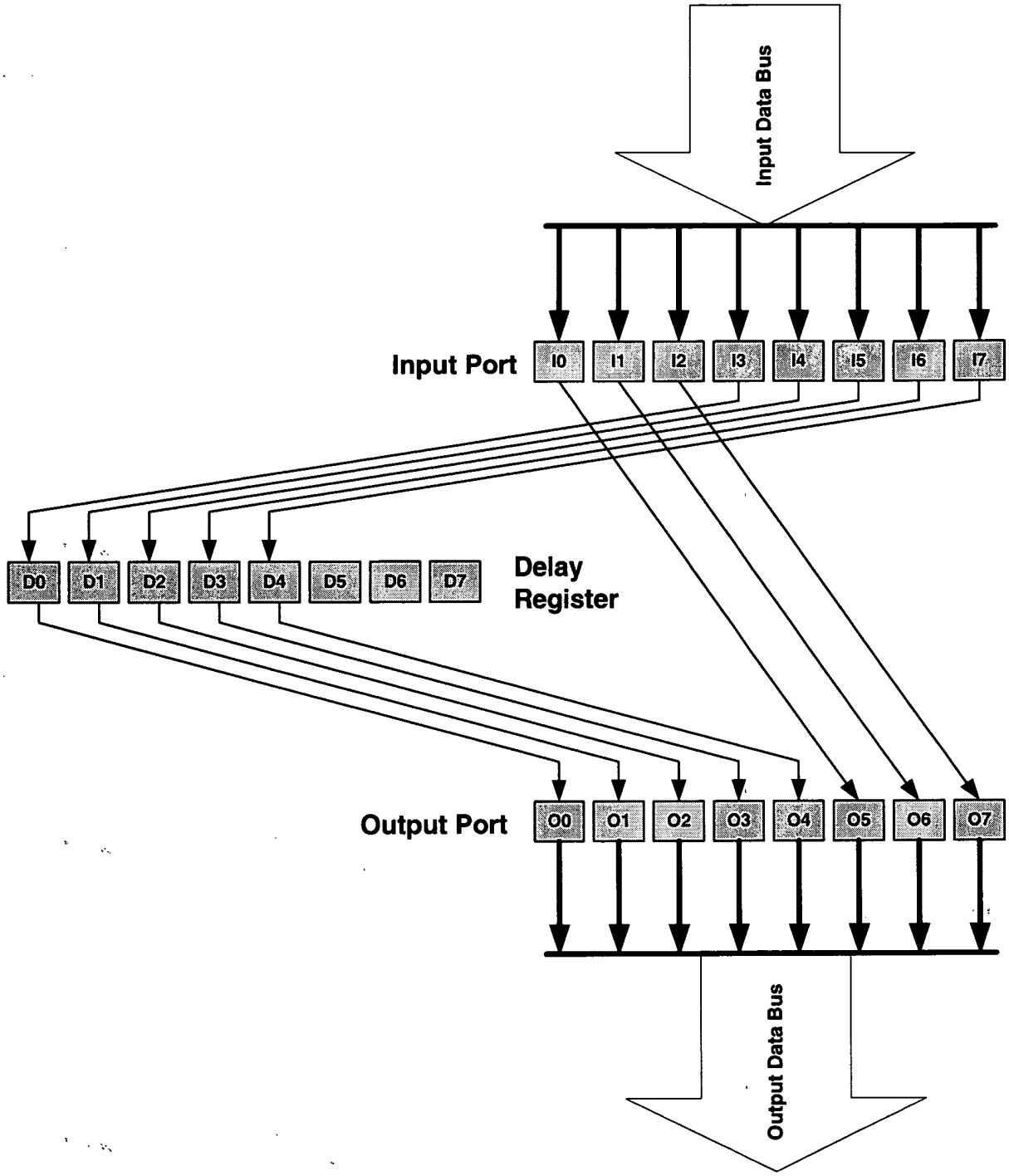
Input Data Bus
Input Port
I0
I1
I2
I3
I4
I5
I6
I7
D0
D1
D2
D3
D4
D5
D6
D7
Delay Register
Output Port
O0
O1
O2
O3
O4
O5
O6
O7
Output Data Bus

FIG. 5

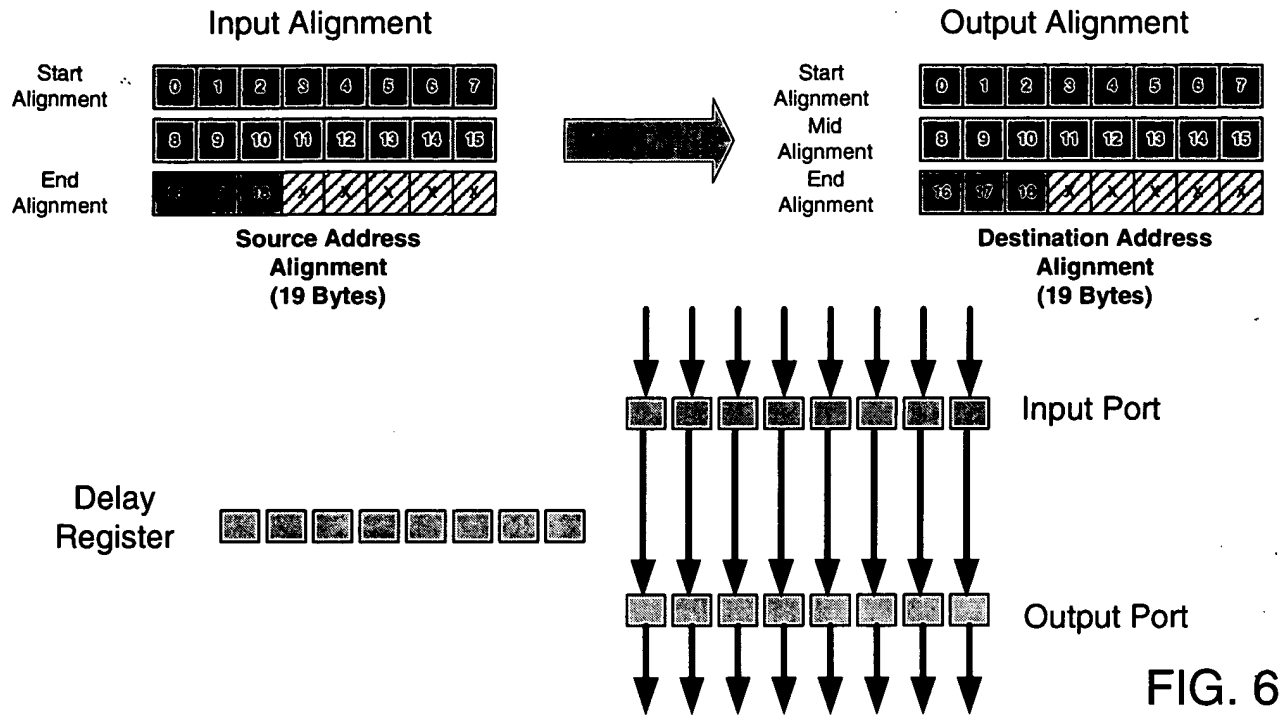
Input Alignment
Start Alignment
End Alignment
Source Address Alignment (19 Bytes)
Output Alignment
Start Alignment
Mid Alignment
End Alignment
Destination Address Alignment (19 Bytes)
Input Port
Delay Register
Output Port

FIG. 6

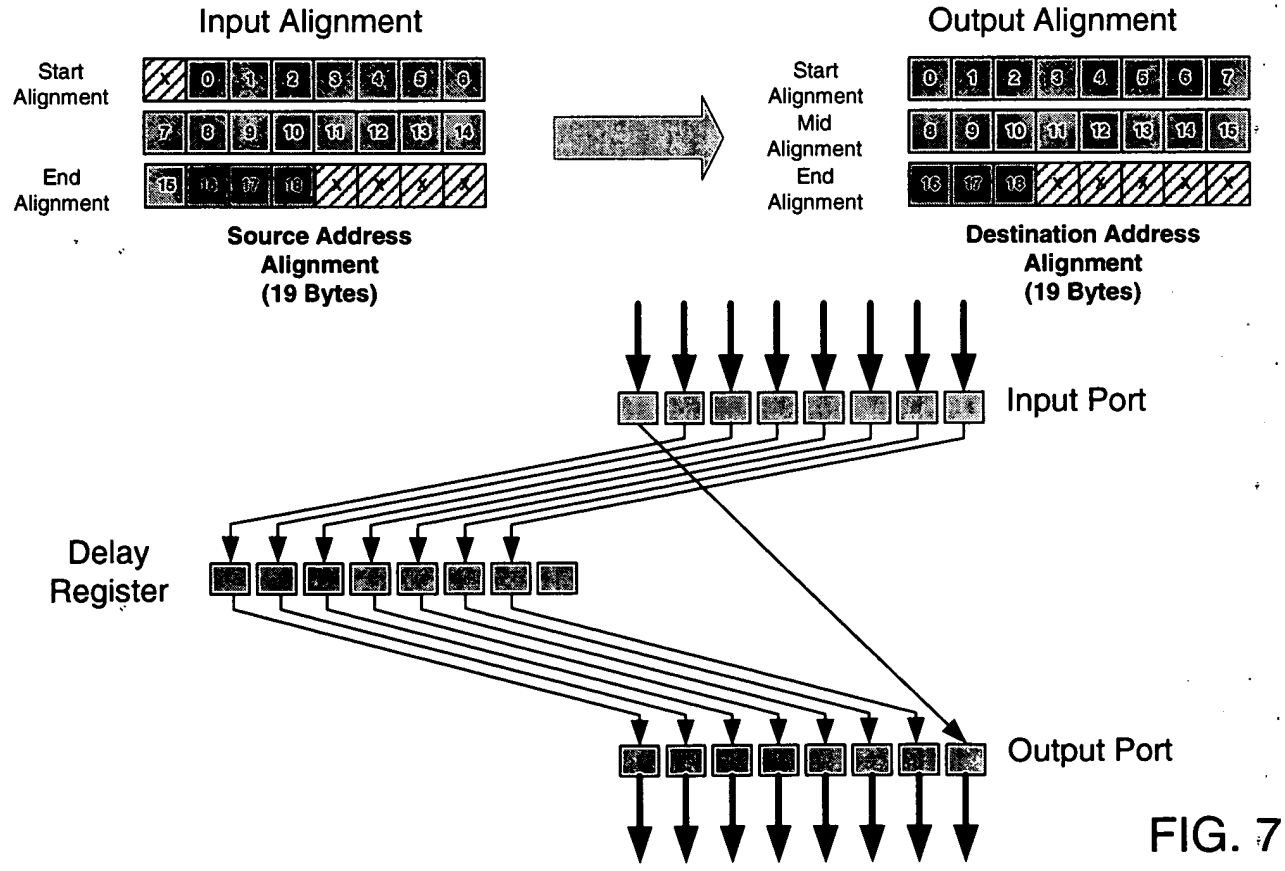
Input Alignment
Start Alignment
End Alignment
Source Address Alignment (19 Bytes)
Output Alignment
Start Alignment
Mid Alignment
End Alignment
Destination Address Alignment (19 Bytes)
Input Port
Delay Register
Output Port

FIG. 7

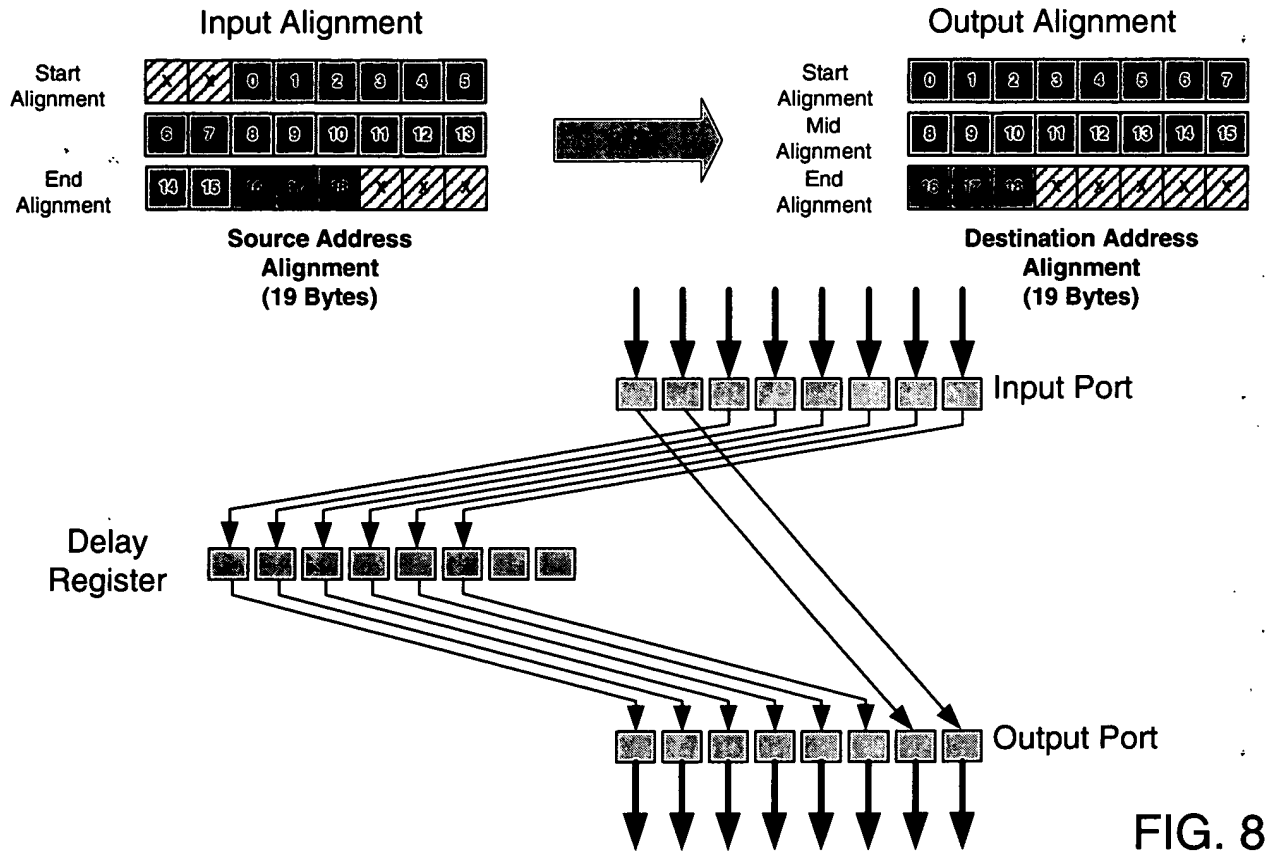
Input Alignment
Start Alignment
End Alignment
Source Address Alignment (19 Bytes)
Output Alignment
Start Alignment
Mid Alignment
End Alignment
Destination Address Alignment (19 Bytes)
Input Port
Delay Register
Output Port

FIG. 8

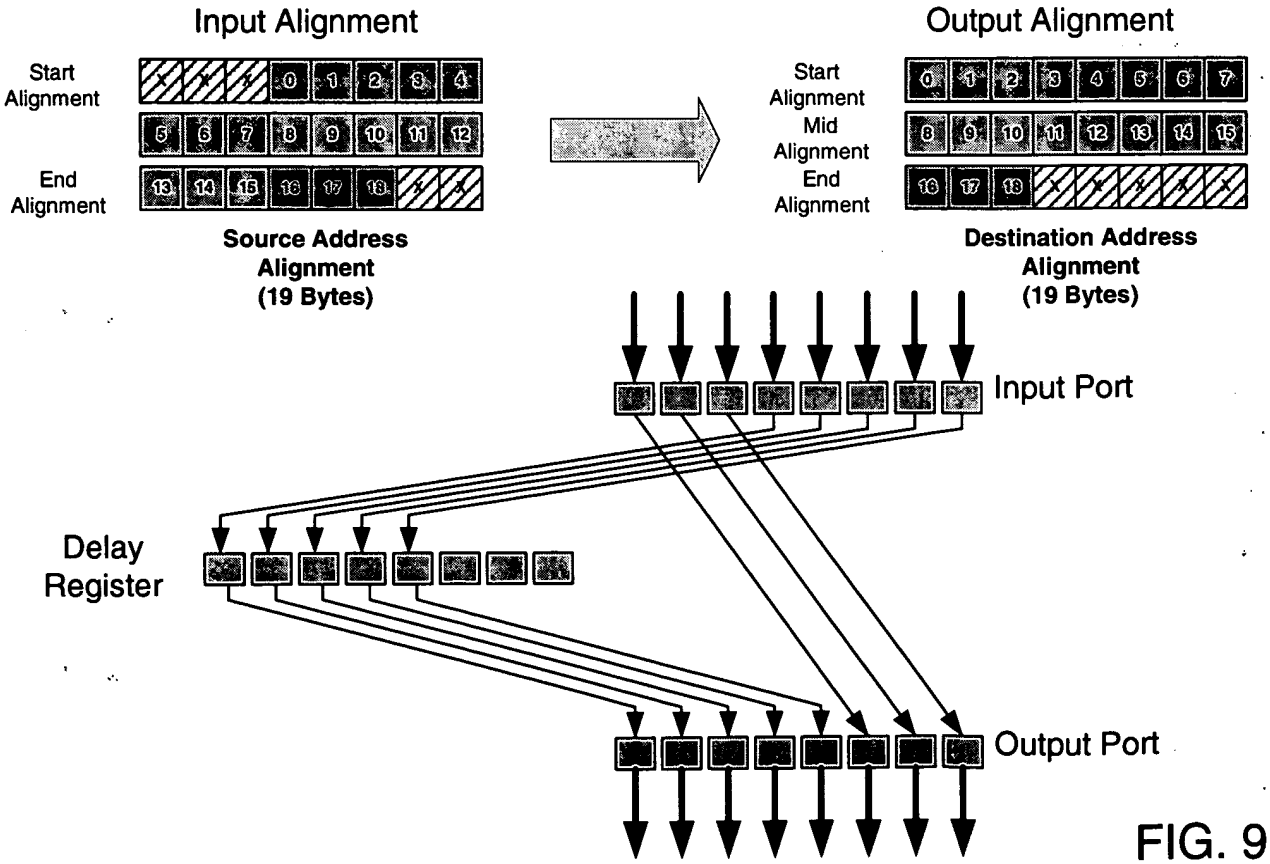
Input Alignment
Start Alignment
End Alignment
Source Address Alignment (19 Bytes)
Output Alignment
Start Alignment
Mid Alignment
End Alignment
Destination Address Alignment (19 Bytes)
Input Port
Delay Register
Output Port

FIG. 9

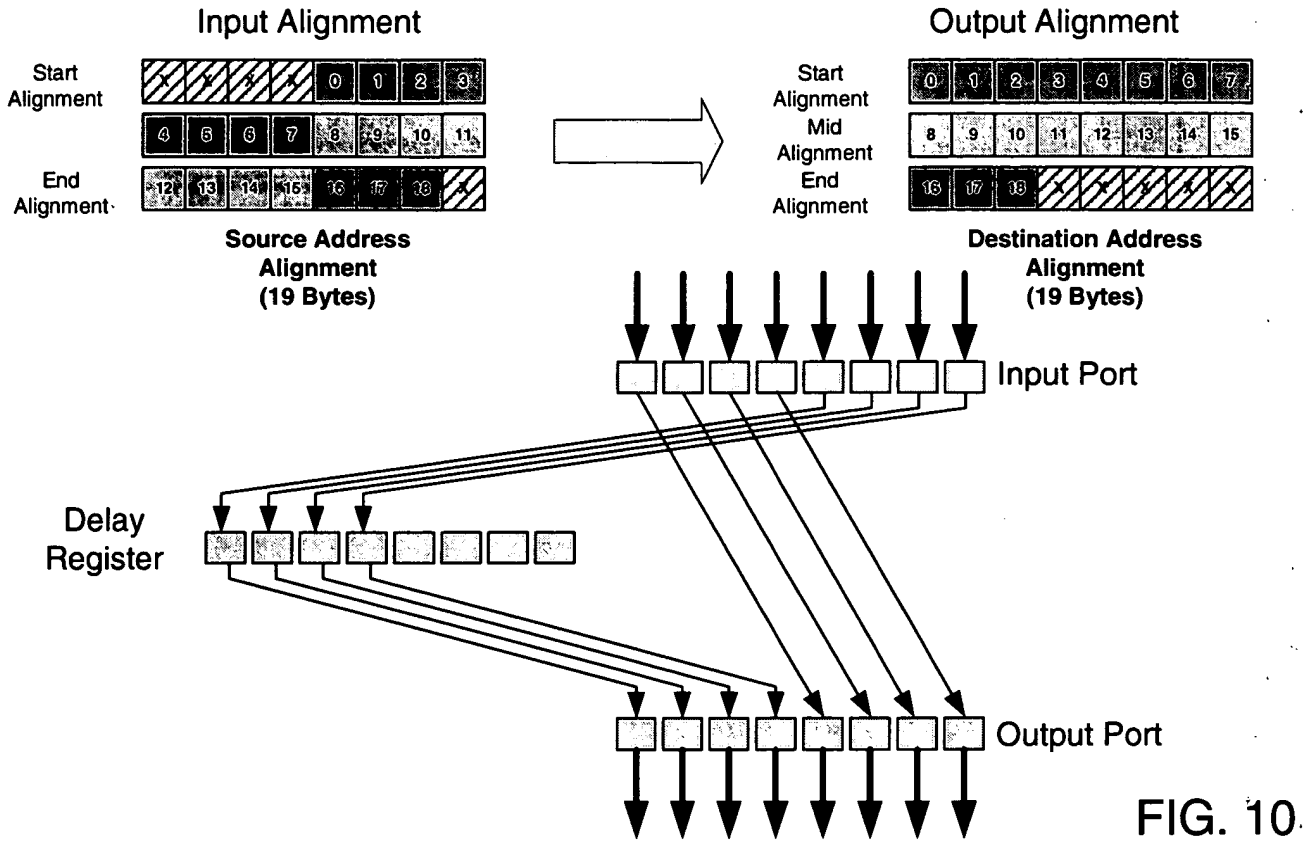
Input Alignment
Start Alignment
End Alignment
Source Address Alignment (19 Bytes)
Output Alignment
Start Alignment
Mid Alignment
End Alignment
Destination Address Alignment (19 Bytes)
Input Port
Delay Register
Output Port

FIG. 10

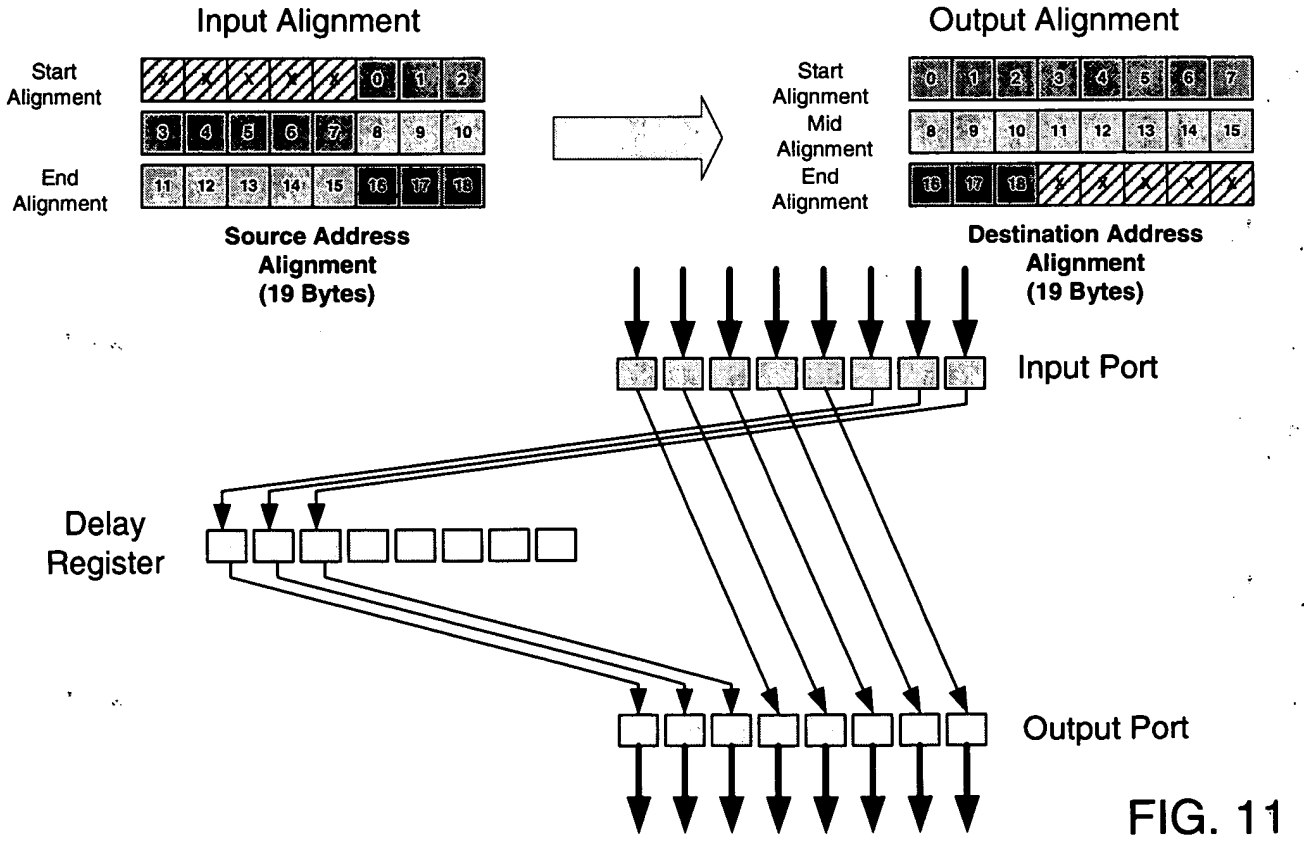
Input Alignment
Start Alignment
End Alignment
Source Address Alignment (19 Bytes)
Output Alignment
Start Alignment
Mid Alignment
End Alignment
Destination Address Alignment (19 Bytes)
Input Port
Delay Register
Output Port

FIG. 11

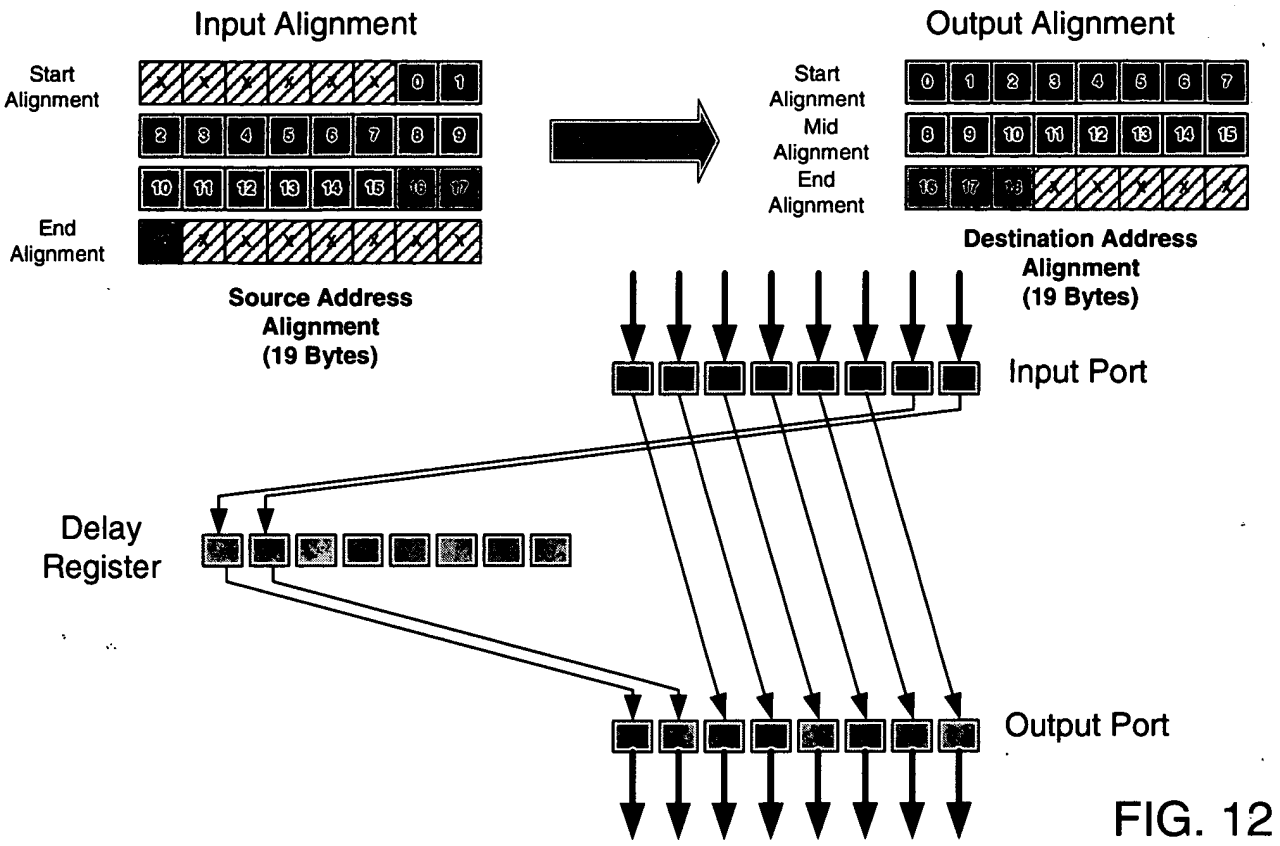
Input Alignment
Start Alignment
End Alignment
Source Address Alignment (19 Bytes)
Output Alignment
Start Alignment
Mid Alignment
End Alignment
Destination Address Alignment (19 Bytes)
Input Port
Delay Register
Output Port

FIG. 12

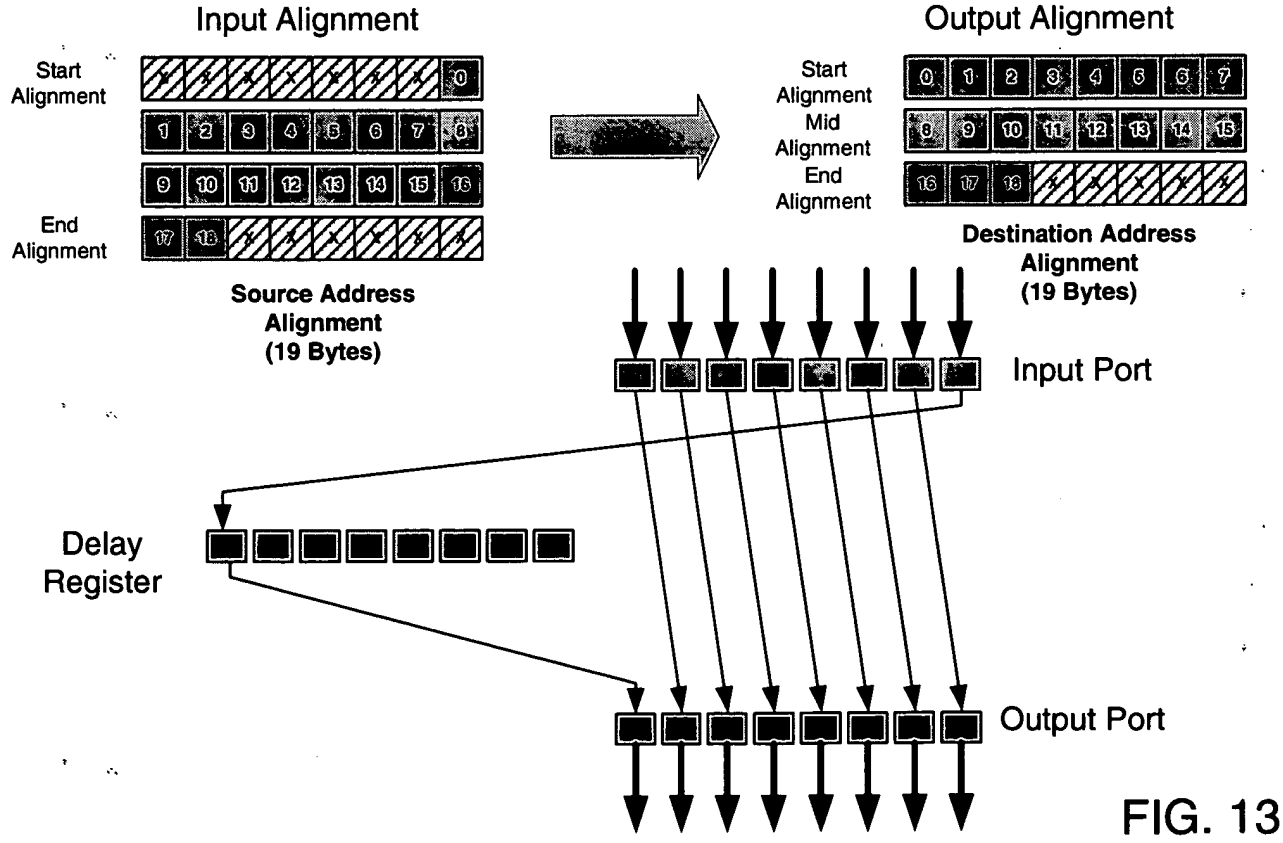
Input Alignment
Start Alignment
End Alignment
Source Address Alignment (19 Bytes)
Output Alignment
Start Alignment
Mid Alignment
End Alignment
Destination Address Alignment (19 Bytes)
Input Port
Delay Register
Output Port

FIG. 13

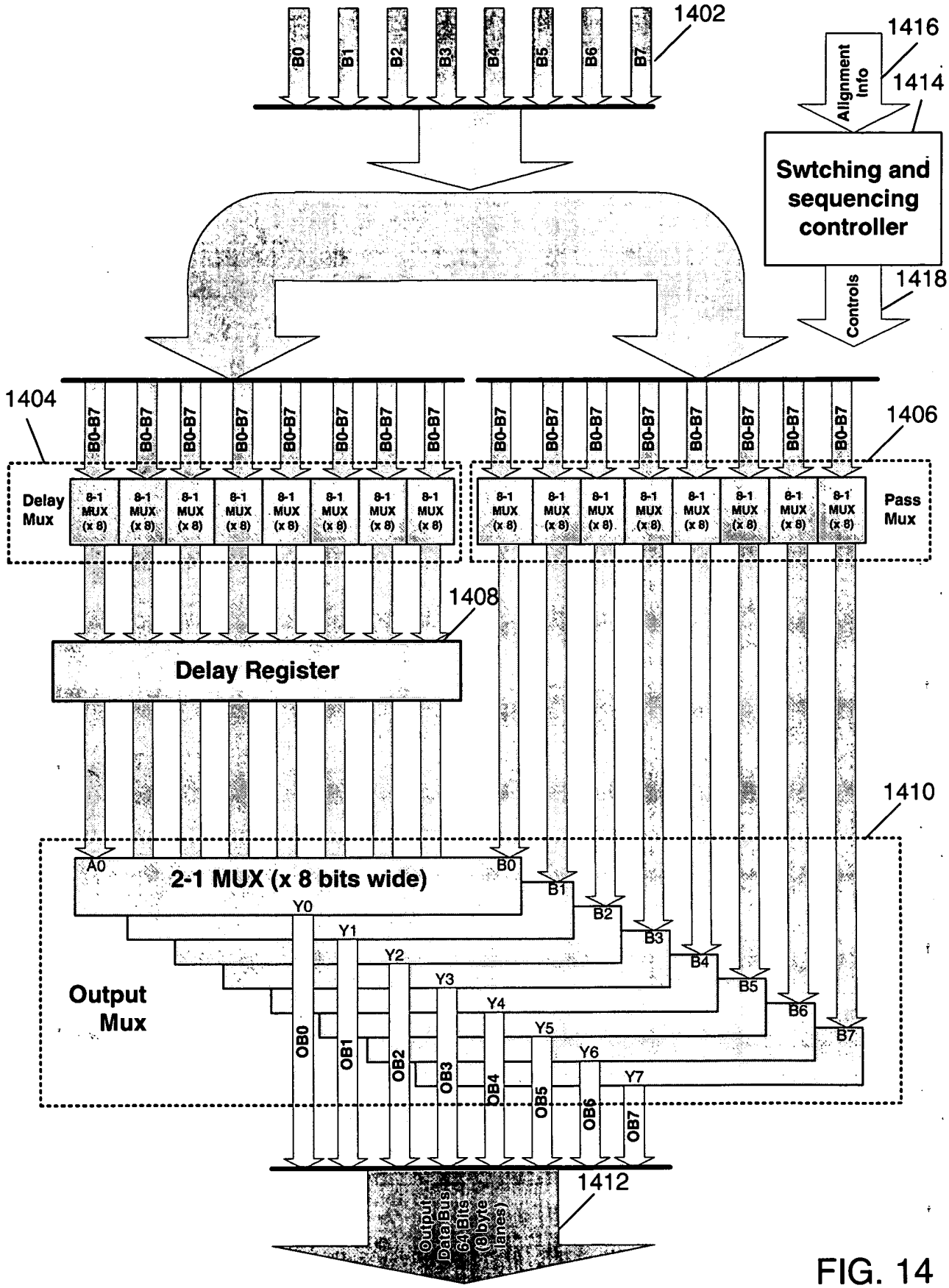
1402
B0
B1
B2
B3
B4
B5
B6
B7
1416
Alignment Info
1414
Swtching and sequencing controller
1418
Controls
1404
1406
B0-B7
Delay Mux
Pass Mux
8-1 MUX (x 8)
1408
Delay Register
1410
A0
B0
2-1 MUX (x 8 bits wide)
Y0
Y1
Y2
Y3
Y4
Y5
Y6
Y7
Output Mux
OB0
OB1
OB2
OB3
OB4
OB5
OB6
OB7
1412
Output Data Bus 64 Bits (8 byte lanes)

FIG. 14

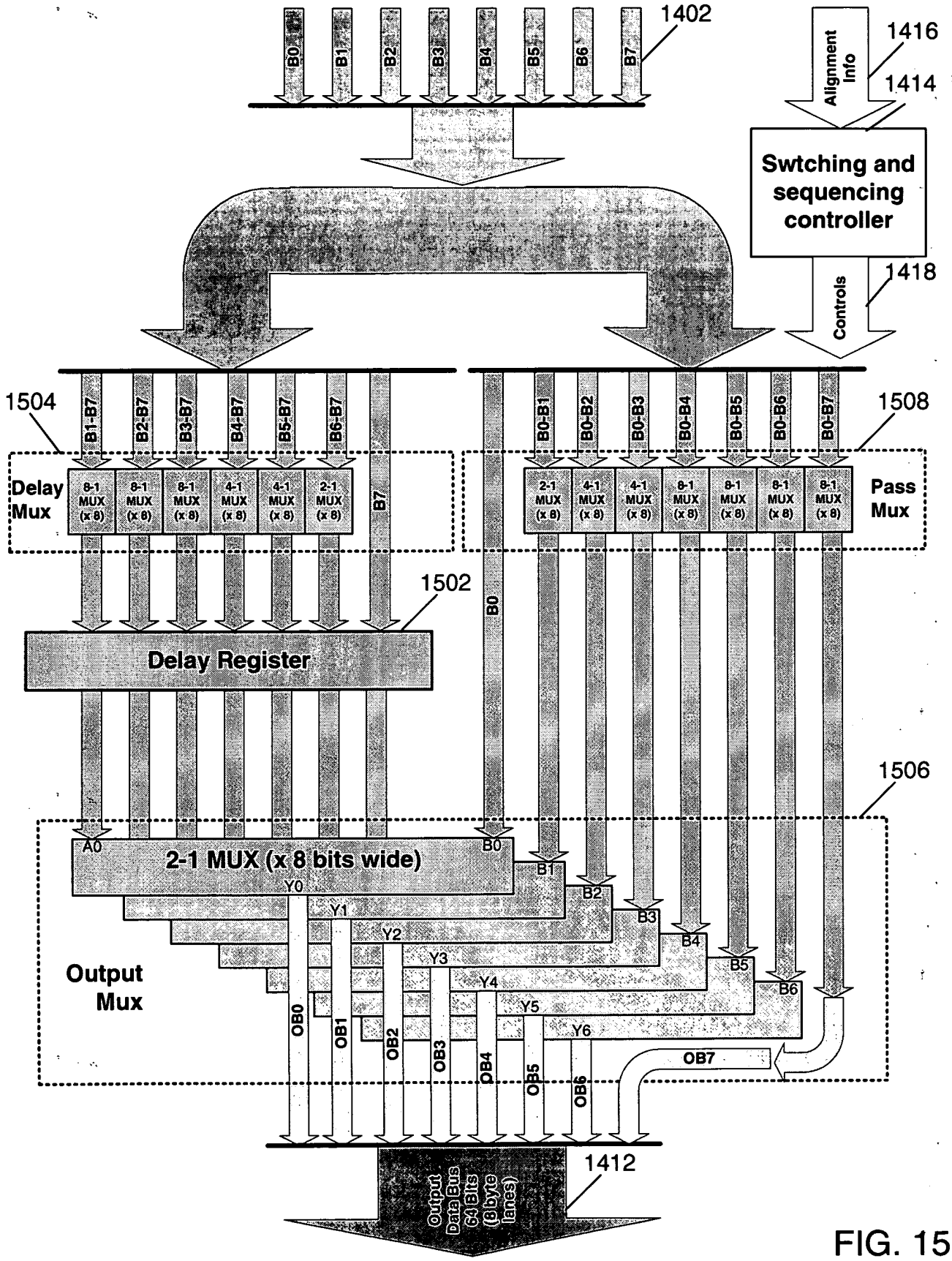
1402
B0
B1
B2
B3
B4
B5
B6
B7
1416
Alignment Info
1414
Swtching and sequencing controller
1418
Controls
1504
1508
B1-B7
B2-B7
B3-B7
B4-B7
B5-B7
B6-B7
B0-B1
B0-B2
B0-B3
B0-B4
B0-B5
B0-B6
B0-B7
Delay Mux
Pass Mux
8-1 MUX (x 8)
4-1 MUX (x 8)
2-1 MUX (x 8)
1502
Delay Register
1506
A0
2-1 MUX (x 8 bits wide)
Y0
Y1
Y2
Y3
Y4
Y5
Y6
Output Mux
OB0
OB1
OB2
OB3
OB4
OB5
OB6
OB7
1412
Output Data Bus 64 Bits (8 byte lanes)

FIG. 15

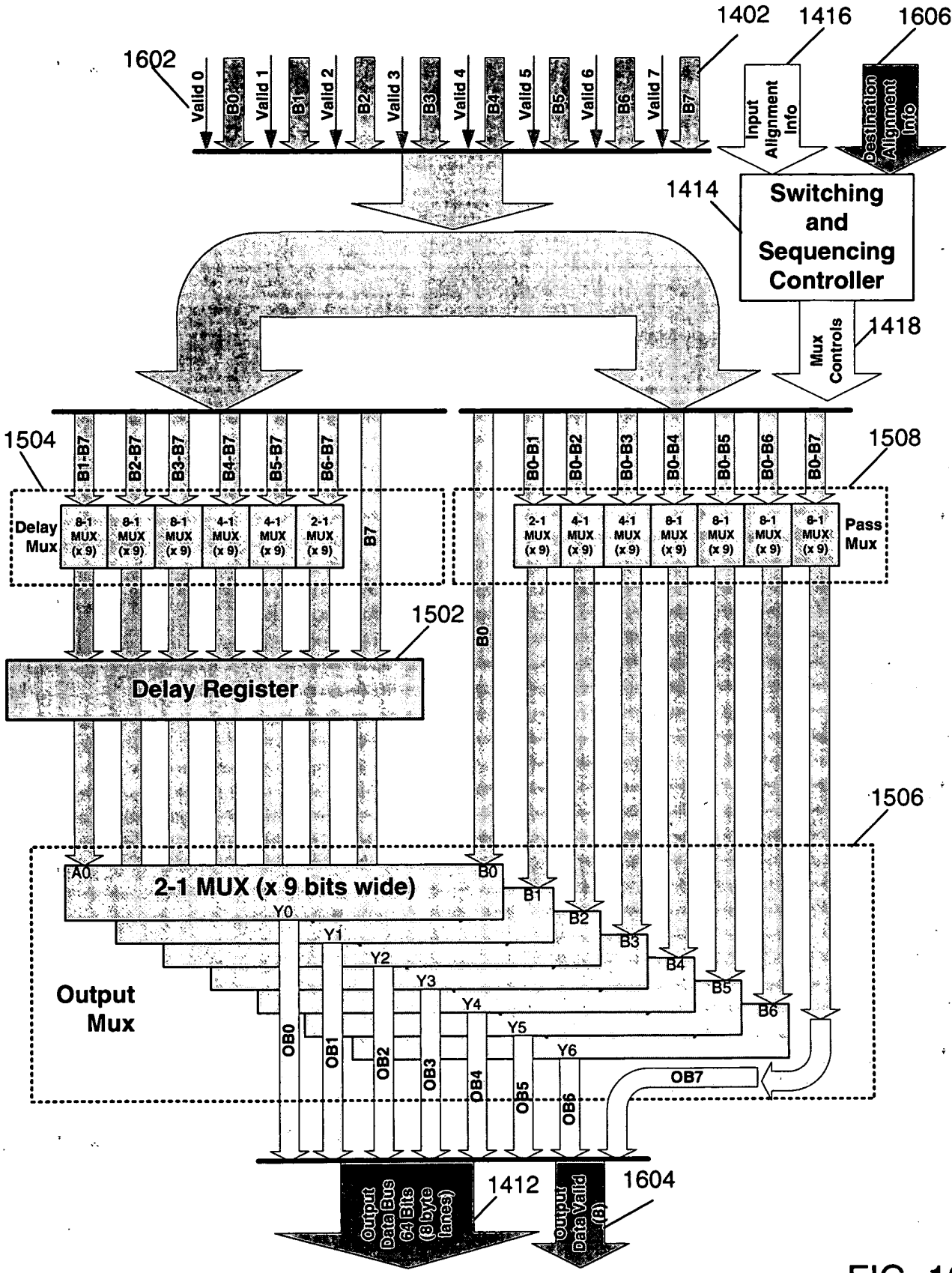
1602
1402
1416
1606
Valid 0
B0
Valid 1
B1
Valid 2
B2
Valid 3
B3
Valid 4
B4
Valid 5
B5
Valid 6
B6
Valid 7
B7
Input Alignment Info
Destination Alignment Info
1414
Switching and Sequencing Controller
Mux Controls
1418
1504
1508
B1-B7
B2-B7
B3-B7
B4-B7
B5-B7
B6-B7
B0-B1
B0-B2
B0-B3
B0-B4
B0-B5
B0-B6
B0-B7
Delay Mux
8-1 MUX (x 9)
4-1 MUX (x 9)
2-1 MUX (x 9)
Pass Mux
1502
Delay Register
1506
A0
2-1 MUX (x 9 bits wide)
Y0
Y1
Y2
Y3
Y4
Y5
Y6
Output Mux
OB0
OB1
OB2
OB3
OB4
OB5
OB6
OB7
Output Data Bus 64 Bits (8 byte lanes)
1412
Output Data Valid (8)
1604

FIG. 16

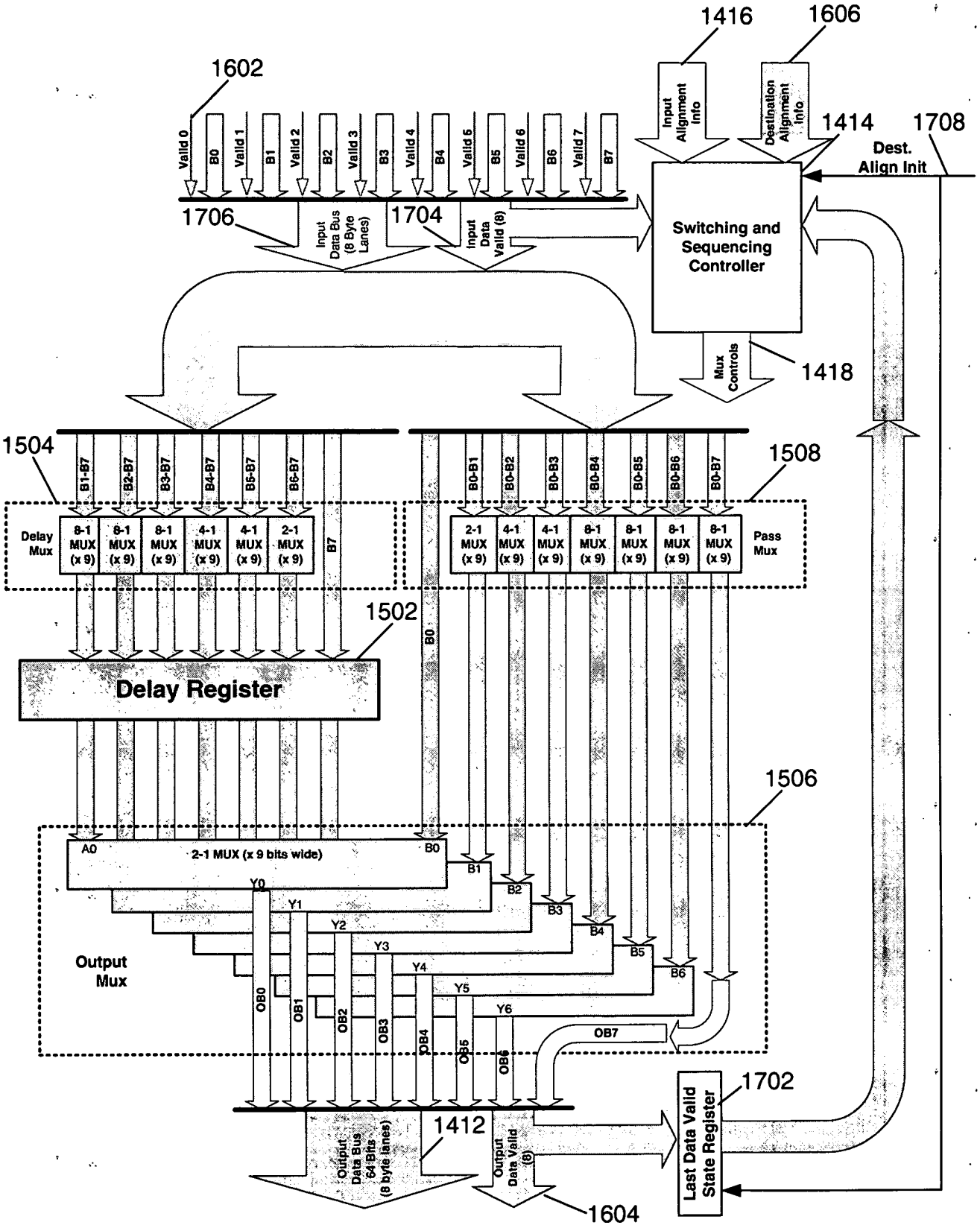
1602
1416
1606
1414
1708
Dest. Align Init
Input Alignment Info
Destination Alignment Info
Valid 0
B0
Valid 1
B1
Valid 2
B2
Valid 3
B3
Valid 4
B4
Valid 5
B5
Valid 6
B6
Valid 7
B7
1706
1704
Input Data Bus (8 Byte Lanes)
Input Data Valid (8)
Switching and Sequencing Controller
Mux Controls
1418
1504
1508
B1-B7
B2-B7
B3-B7
B4-B7
B5-B7
B6-B7
B0-B1
B0-B2
B0-B3
B0-B4
B0-B5
B0-B6
B0-B7
Delay Mux
8-1 MUX (x 9)
8-1 MUX (x 9)
8-1 MUX (x 9)
4-1 MUX (x 9)
4-1 MUX (x 9)
2-1 MUX (x 9)
B7
2-1 MUX (x 9)
4-1 MUX (x 9)
4-1 MUX (x 9)
8-1 MUX (x 9)
8-1 MUX (x 9)
8-1 MUX (x 9)
8-1 MUX (x 9)
Pass Mux
1502
B0
Delay Register
1506
A0
2-1 MUX (x 9 bits wide)
B0
B1
B2
B3
B4
B5
B6
Y0
Y1
Y2
Y3
Y4
Y5
Y6
OB7
Output Mux
OB0
OB1
OB2
OB3
OB4
OB5
OB6
1412
Output Data Bus 64 Bits (8 byte lanes)
Output Data Valid (8)
1702
Last Data Valid State Register
1604

FIG. 17

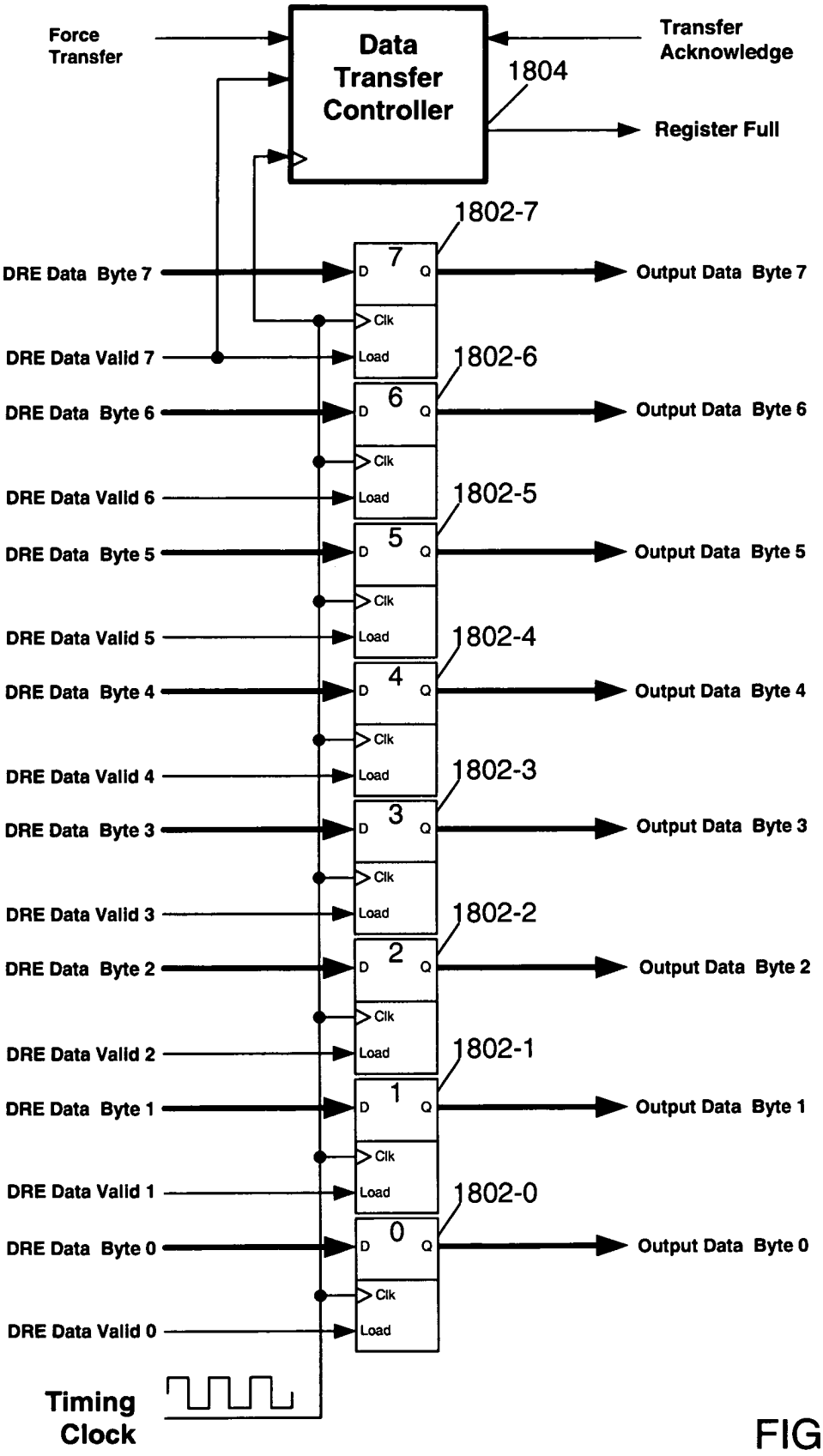
Force Transfer
Data Transfer Controller
1804
Transfer Acknowledge
Register Full
1802-7
DRE Data Byte 7
7
D
Q
Output Data Byte 7
Clk
DRE Data Valid 7
Load
1802-6
DRE Data Byte 6
6
Output Data Byte 6
DRE Data Valid 6
1802-5
DRE Data Byte 5
5
Output Data Byte 5
DRE Data Valid 5
1802-4
DRE Data Byte 4
4
Output Data Byte 4
DRE Data Valid 4
1802-3
DRE Data Byte 3
3
Output Data Byte 3
DRE Data Valid 3
1802-2
DRE Data Byte 2
2
Output Data Byte 2
DRE Data Valid 2
1802-1
DRE Data Byte 1
1
Output Data Byte 1
DRE Data Valid 1
1802-0
DRE Data Byte 0
0
Output Data Byte 0
DRE Data Valid 0
Timing Clock

FIG. 18

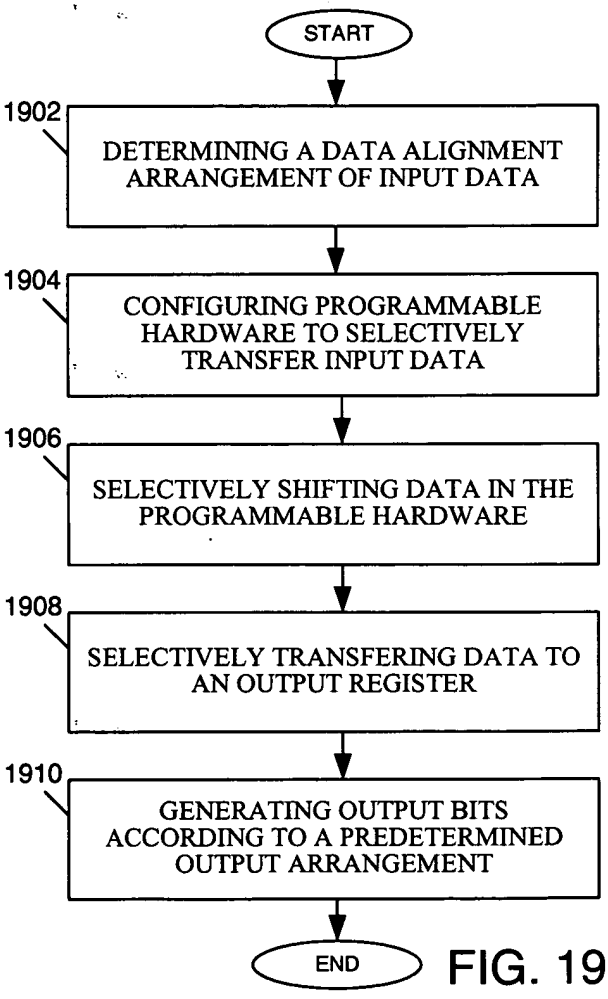
START
1902
DETERMINING A DATA ALIGNMENT ARRANGEMENT OF INPUT DATA
1904
CONFIGURING PROGRAMMABLE HARDWARE TO SELECTIVELY TRANSFER INPUT DATA
1906
SELECTIVELY SHIFTING DATA IN THE PROGRAMMABLE HARDWARE
1908
SELECTIVELY TRANSFERING DATA TO AN OUTPUT REGISTER
1910
GENERATING OUTPUT BITS ACCORDING TO A PREDETERMINED OUTPUT ARRANGEMENT
END

FIG. 19

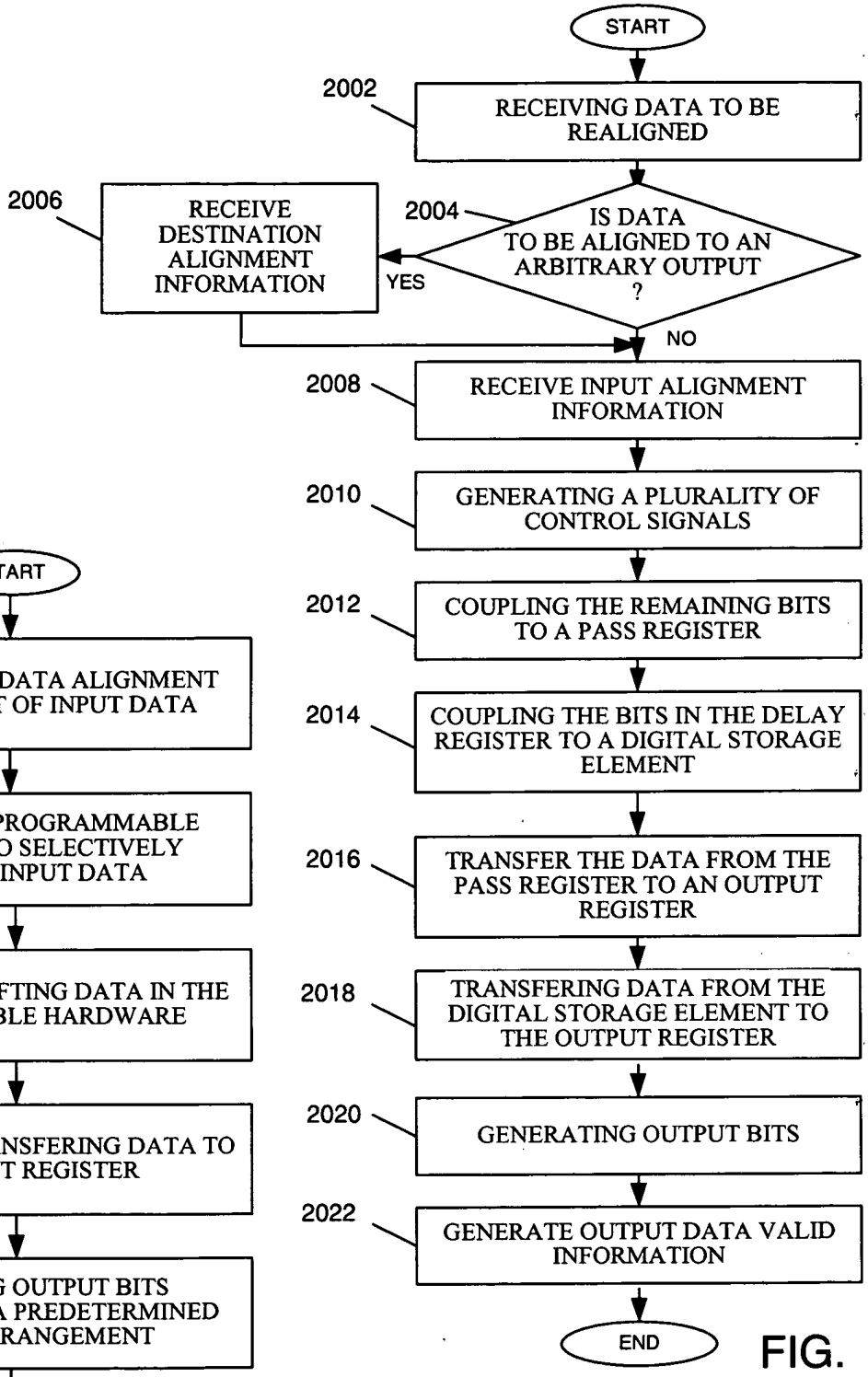
START
2002
RECEIVING DATA TO BE REALIGNED
2004
IS DATA TO BE ALIGNED TO AN ARBITRARY OUTPUT ?
YES
2006
RECEIVE DESTINATION ALIGNMENT INFORMATION
NO
2008
RECEIVE INPUT ALIGNMENT INFORMATION
2010
GENERATING A PLURALITY OF CONTROL SIGNALS
2012
COUPLING THE REMAINING BITS TO A PASS REGISTER
2014
COUPLING THE BITS IN THE DELAY REGISTER TO A DIGITAL STORAGE ELEMENT
2016
TRANSFER THE DATA FROM THE PASS REGISTER TO AN OUTPUT REGISTER
2018
TRANSFERING DATA FROM THE DIGITAL STORAGE ELEMENT TO THE OUTPUT REGISTER
2020
GENERATING OUTPUT BITS
2022
GENERATE OUTPUT DATA VALID INFORMATION
END

FIG. 20

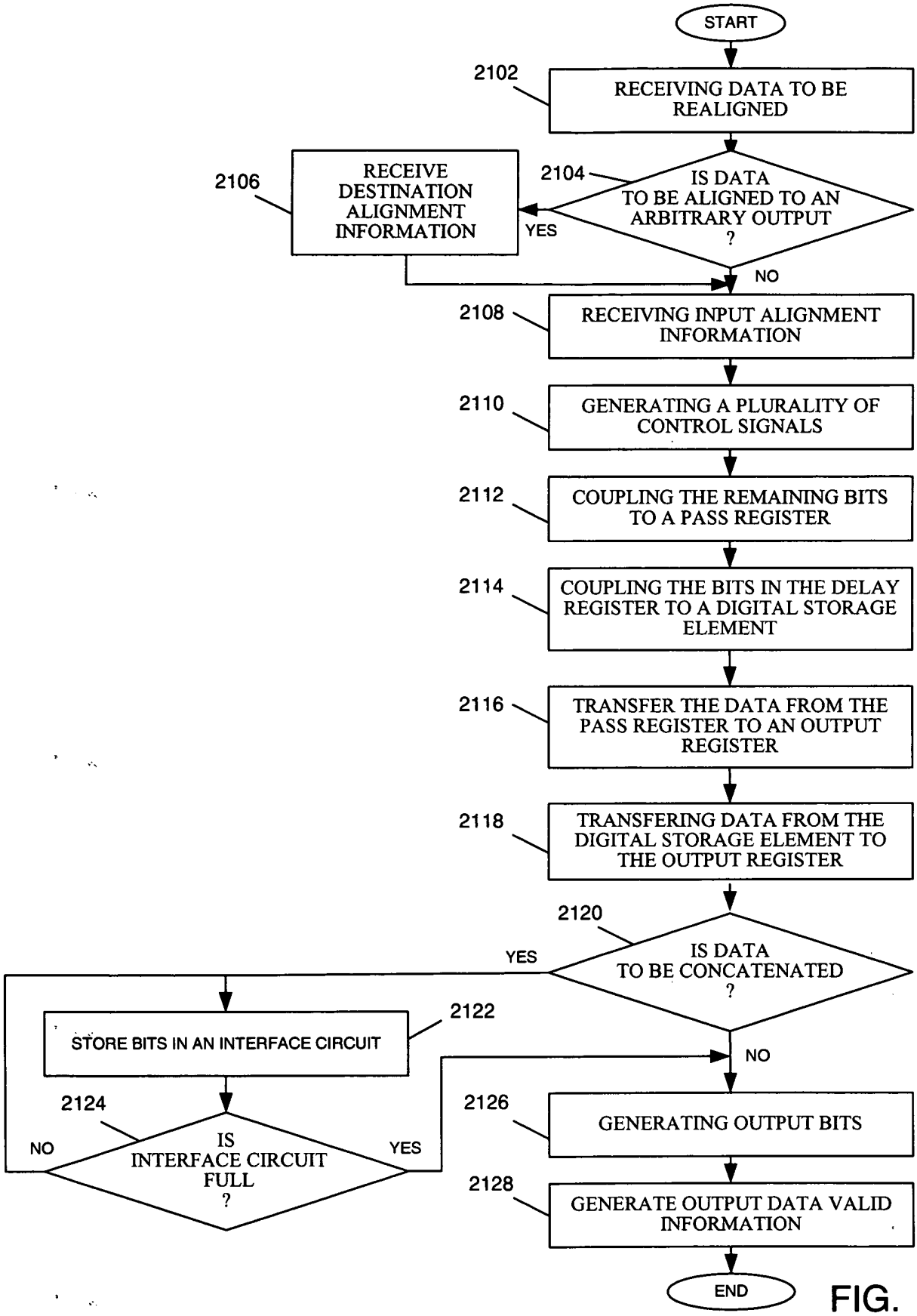
START
2102
RECEIVING DATA TO BE REALIGNED
2104
IS DATA TO BE ALIGNED TO AN ARBITRARY OUTPUT ?
YES
2106
RECEIVE DESTINATION ALIGNMENT INFORMATION
NO
2108
RECEIVING INPUT ALIGNMENT INFORMATION
2110
GENERATING A PLURALITY OF CONTROL SIGNALS
2112
COUPLING THE REMAINING BITS TO A PASS REGISTER
2114
COUPLING THE BITS IN THE DELAY REGISTER TO A DIGITAL STORAGE ELEMENT
2116
TRANSFER THE DATA FROM THE PASS REGISTER TO AN OUTPUT REGISTER
2118
TRANSFERING DATA FROM THE DIGITAL STORAGE ELEMENT TO THE OUTPUT REGISTER
2120
IS DATA TO BE CONCATENATED ?
YES
2122
STORE BITS IN AN INTERFACE CIRCUIT
2124
IS INTERFACE CIRCUIT FULL ?
NO
YES
NO
2126
GENERATING OUTPUT BITS
2128
GENERATE OUTPUT DATA VALID INFORMATION
END

FIG. 21